

Application Serial No.: 10/625,513  
Reply to Office Action dated June 29, 2004

**REMARKS/ARGUMENTS**

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-4 are pending in this application.

The outstanding Office Action includes an objection to the title and a rejection of Claims 1-4 under 35 U.S.C. §103(a) as being unpatentable over Ryuichi et al. (JP 10-209272, Ryuichi) in view of Fitch et al. (U.S. Patent No. 5,554,870, Fitch).

The objection to the title is also believed to be moot in view of the amended title submitted herewith that is clearly more descriptive of the claimed invention.

Before considering the outstanding art rejection, it is believed that a brief review of the present invention would be helpful. In this regard, the present invention includes a lower level interconnect structure that has at least conductive interconnect body portion with a topside conductive film exposed in a contact hole serving as a via through an interlayer insulating film. The conductive interconnect body is provided with a high resistance layer on a side end face thereof also exposed in the contact hole to separate the side surface of the conductive interconnect body from a via plug then formed the contact hole.

Alternatively, the side end face of the conductive interconnect body portion is withdrawn underneath an overhanging portion of the topside conductive film to form a withdrawn end face. A portion of the interlayer insulating film fills the space formed between the withdrawn end face and a projected end face of the overhanging portion of the

topside conductive film so as to separate the withdrawn end face and a conductive plug formed in the contact hole.

In either of the above alternative approaches of separating the end face of the conductive interconnect body portion in the contact hole from the conductive plug in the contact hole, a current concentration that can occur if the end surface of the conductive interconnect body and the conductive via plug are in contact is prevented. Note the specification at page 2, lines 13-22, for example.

Turning to Ryuichi, it is clear that the showing of Fig. 10 only teaches the process and structure described at page 1, line 11 through page 2, line 12, of the description of the background art portion of the specification of this application. As noted at page 2, lines 13-22, of the specification, this conventional Ryuichi device and method have been determined by the present applicants to invite the above-noted undesirable current concentration in the region where the side surface portion of the lower-level conductive interconnect body are connected.

As shown in Fig. 10 of Ryuichi, a part of the side surface of the interconnect body and the via are connected directly to each other and other portions thereof are closely adjacent to each other through the void.

In such a configuration, current concentration can occur in the above mentioned part or discharge can take place via the void, and, consequently, current concentration occurs. That is, Ryuichi does not have the effect of suppressing current concentration.

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Furthermore, in Ryuichi, a high resistance layer does not exist between the side surface of the interconnect body and the via.

On the other hand, Fitch teaches a completely different integrated circuit structure having a channel region 30 that is formed in an opening etched through the dielectric layer 20 that is over the conductive layer 18 on top of the dielectric layer 16. The layer 18 is laterally etched, as described at col. 4, lines 40-45, so that a dielectric layer 22' can be added to function as a gate dielectric as noted at col. 4, lines 58-60. Thus, the Fitch teaching is that the conductive layer 18 is to function as a gate separated from the channel region 30 in the opening by the gate dielectric 22' as further described at col. 5, lines 46-55.

These Fitch teachings clearly have no relevance to the above-noted teachings of Ryuichi involving a region where the side surface portion of a lower-level conductive interconnect body is connected with a conductive plug in a contact hole and a top conductive layer of the interconnect structure is also connected to the same conductive plug in the same contact hole. Moreover it is not clear why the outstanding Action asserts that the artisan would be led to use the gate dielectric 22' with the Ryuichi device to reduce or resist plasma damage as urged at page 3 of the outstanding Action.

While col.4, lines 60-64, of Fitch teach that the dielectric layer 22' is nitrided so this gate dielectric itself can better resist plasma damage, this is to insure better performance as a gate dielectric and has nothing to do with the Ryuichi contact of the interconnect structure to a conductive plug in a contact hole.

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Accordingly, as it is clear that the PTO has not properly explained why the artisan would seek to modify the dissimilar interconnect structure of Ryuich by the gate-gate dielectric-channel teachings of Fitch, or why these references would even be selected for a combination, and, accordingly the rejection is improper and traversed. See In re Rouffet, 47 USPQ2d 1453, 1459 (Fed. Cir. 1998) and note the requirement therein for the PTO to explain the reasons why one of ordinary skill in the art would have been motivated to select clearly disparate references and then to attempt to combine their clearly disparate teachings.

If the PTO is to continue to suggest that the artisan would seek to modify the dissimilar interconnect structure of Ryuich by the gate-gate dielectric-channel teachings of Fitch, to arrive at the subject matter of independent Claim 1, it is called upon to present the “full and reasoned explanation” required by In re Lee, 61 USPQ2d 1430, 1432-33 (Fed. Cir. 2002). Also note the requirement of In re Rijckaert, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993) that if “the PTO asserts that there is an explicit or implicit teaching or suggestion in the prior art, it must indicate where such a teaching or suggestion appears in the reference.”

As Claims 2 and 3 depend from Claim 1, the rejection thereof as being unpatentable over Ryuichi in view of Fitch is traversed for the reasons noted above as to Claim 1. In addition, the product by process limitations of these claims lead to specific structure in terms of the composition of the high resistance layer shared with Claim 1 and the outstanding Action fails to address these different types of high resistance layers. Thus, the rejection of Claims 2 and 3 is traversed for this reason as well.

Turning to independent Claim 4, this claim requires, *inter alia*, “a portion of said interlayer insulating film” to be in the “space” formed between the withdrawn end face of the interconnect body under the conductive film and “the second region of said conductor” in the “contact hole extending through said interlayer insulating film.” Whatever else can be said of layer 22’ of Fitch, it is clearly NOT “a portion of said interlayer insulating film” that the opening is formed in as this can only be read on the insulating layer 20 of Fitch. In this regard, 22’ is not “a portion” of either insulating layer 20 or insulating layer 16.

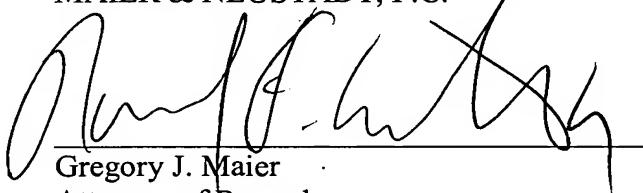
Thus, even if the artisan had some unknown reason to modify the dissimilar interconnect structure of Ryuich by the gate-gate dielectric-channel teachings of Fitch, he still would not arrive at the subject matter of independent Claim 4 as the layer 22’ would be a layer separate from any of layers 20, 18, and 16 of Fitch, or the layer 3 of Ryuich. Accordingly, the rejection of Claim 4 is traversed for this reason as well as for the lack of establishment of the required showing of reasonable motivation to even attempt to combine these references as fully set forth above as to Claim 1.

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Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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